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Attorney Reference Number 6319-56134

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Box PATENT APPLICATION
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Washington, D.C. 20231

24197

Transmitted herewith for filing is the patent application of:

Inventor(s): Chin-Huang Chang

For: METHOD FOR REDUCING SIZE OF SEMICONDUCTOR UNIT IN PACKAGING PROCESS

Enclosed are:

☒ 10 pages of specification, 4 pages of claims, an abstract and a Combined Declaration and Power of Attorney.
☒ 4 sheet(s) of formal drawings.
☒ An assignment of the invention to: Silicon Precision Industries Co., Ltd. and a Recordation Cover Sheet.

FILING FEE

For	Claims Filed	Number Free		Number Extra	Rate	Basic Fee $690.00
Total Claims	20	20	=	0	$18.00	$ 0.00
Independent Claims	3	3	=	0	$78.00	$ 0.00
Multiple Dependent Claim Fee					$260.00	$0.00
TOTAL FILING FEE						$690.00

☒ A check in the amount of $730.00 to cover ☒ filing fee and ☒ assignment recordal fee is enclosed.

☒ The Director is hereby authorized to charge any additional fees which may be required in connection with the filing of this application and recording any assignment filed herewith, or credit over-payment, to Account No. 02-4550. A copy of this sheet is enclosed.

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Respectfully submitted,

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METHOD FOR REDUCING SIZE OF SEMICONDUCTOR UNIT IN PACKAGING PROCESS

FIELD OF THE INVENTION

The present invention relates to schemes of reducing the size of at least a semiconductor unit, particularly to technologies of reducing the size of at least a semiconductor unit in packaging the semiconductor unit.

BACKGROUND OF THE INVENTION

In conventional processes of packaging an IC chip, back-side grinding of a wafer is the first step which is followed by wafer sawing to divide a wafer into a plurality of dice, and the dice are then attached to substrates. According to such conventional processes, grinding on the basis of mechanical force is still applied to a chip even when the thickness of the chip approximates an expected specification, resulting in the fact that the chip tends to suffer from back-side chipping. This result is particularly serious in case the expected specification of the thickness of the chip is relatively small. Furthermore, a chip so ground as to have a critical thickness (such as 6 mil or below) tends to suffer from die crack, and the process of back-side grinding of a chip, particularly when the thickness of the chip approximates the expected specification, always involves petty but indispensable procedures. It can thus be concluded that the cost optimization for such conventional IC packaging processes and the quality stabilization of product therein can never be realized due to the need thereof for complicated and petty procedures, and the significant failure rate inherent therein resulting from back-side chipping and die crack.

To provide solutions to the above problems which are associated with conventional chip packaging processes, the present invention

develops new schemes for reducing the size of a chip, which features replacing conventional back-grinding of a chip by the etching on a surface of the chip, particularly during the phase the thickness of the chip reaches a range of 8～10 mil, thereby the failure rate of process of packaging at least a chip can be significantly lowered, and the petty procedures involved by grinding a thin chip can be abridged.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a method for reducing the size of a semiconductor unit, in order to immunize semiconductor unit packaging processes against the back-side chipping resulting from back-side grinding of a thin chip, and the die crack resulting from sawing a wafer, or handling, or processing, or connecting a chip.

Another object of the present invention is provide a method for reducing the size of a semiconductor unit, in order to eliminate the need of petty procedures in grinding a thin wafer.

A further object of the present invention is to provide different etching modes for industries to select, according to individual product or condition, better scheme for reducing the size of at least a semiconductor unit in the processes of packaging at least a semiconductor unit, thereby the cost of an IC package can be economized, and the stable product quality thereof can be reliably sustained.

The primary difference between the present invention and those conventional arts of packaging a chip is briefed as follows: according to those conventional arts, the size of a chip/die is reduced by grinding on the basis of mechanical force throughout the whole process of packaging a chip/die; while according to the present invention, the size of at least a semiconductor unit is reduced by etching the semiconductor unit,

particularly when the thickness of the semiconductor unit approximates an expected specification (such as the thickness in the range spanning between 8 mil and 10 mil).

The present invention is characterized by using a certain type of gas (plasma, for example) or beams of light to etch at least a thin semiconductor unit until the size of the semiconductor unit meets an expected specification (such as the thickness thereof ranging from 2 mil to 6 mil), thereby IC packaging processes can be immunized against the high failure rate resulting from back-side chipping of a thin chip and die crack.

An aspect of the present invention for reducing the size of at least a semiconductor unit in a process of packaging the semiconductor unit may be a method comprising the steps of:

(A) attaching at least a part of a first surface of the semiconductor unit to a carrier such as a chip carrier (a substrate, for example) or a chip tray ; and

(B) etching the semiconductor unit from a second surface of the semiconductor unit until the size of the semiconductor unit meets an expected specification.

In the process of reducing the size of semiconductor unit according to the above method, the semiconductor unit has its semiconductor electrical connection device such as a pin located on its first surface, and the semiconductor unit may be etched by means selected from among using gas and using beams of light. A preferred embodiment is to etch the semiconductor unit by using plasma.

In the process of reducing the size of semiconductor unit according to the above method, the expected specification may mean that the thickness of the semiconductor unit measured relative to the first surface

is within a specified range, and the specified range may be a range spanning between 2 mil and 6 mil, for example. If the initial thickness of the semiconductor unit is too much larger than the specified range, back-side grinding of the semiconductor unit may be used to reduce the size of the semiconductor unit until the thickness of the semiconductor unit approximates the specified range, such as the range spanning between 8 mil and 10 mil. In the range spanning between 8 mil and 10 mil, grinding on the basis of mechanical force tends to result in high failure rate, and therefore is replaced by the etching process characterizing the present invention.

The above method is suitable for packaging at least a semiconductor unit that, after attaching to the chip carrier, has at least a surface from which the semiconductor unit may be etched. For example, a flip chip with a surface thereof connected with the chip carrier via bumps may have another surface from which the flip chip may be etched, or in a lead-on chip package a chip having part of its first surface stuck to the chip carrier and its bonding wires electrically connected to the chip carrier may have its second surface for etching the chip. The meaning of "attaching" throughout this disclosure includes "placing", and the semiconductor unit may also be properly placed onto a chip tray instead of a chip carrier.

Another aspect of the present invention for reducing the size of at least a semiconductor unit in a process of packaging the semiconductor unit which includes a first surface, a second surface, and at least a semiconductor electrical connection device located on the first surface, may be a method comprising the steps of:

(C) attaching the semiconductor unit to a seating apparatus such as a chip tray, or a chip carrier mechanically or/and electrically connectible

with said semiconductor unit, the first surface thereof facing the seating apparatus and the second surface thereof exposed; and

(D) etching the semiconductor unit from its second surface until the size of the semiconductor unit meets an expected specification, thereby the method provided by the present invention can be suitable for various IC package structures, as can be seen from detailed descriptions hereinafter.

The present invention may best be understood through the following description with reference to the accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows an embodiment of a main step of a method provided by the present invention for reducing the size of a semiconductor unit such as flip chip.

Fig. 2 shows an embodiment of another main step of a method provided by the present invention for reducing the size of a semiconductor unit such as flip chip.

Fig. 3 shows a structure in which a fixture is used to shield those shown in Fig. 1 in order to prevent product quality from being affected by etching process.

Fig. 4 depicts an etching process.

Fig. 5 shows a cross sectional view of the structure where a semiconductor unit has been so etched according to the present invention as to have thickness reaching a range spanning between 2 mil and 6 mil.

Fig. 6 shows a product achieved by reducing the size of a semiconductor unit (such as a flip chip) according to the present invention.

Fig. 7 shows another chip package structure to which the method of reducing the size of at least a semiconductor unit (such as a wire bonding chip) according to the present invention may be applicable.

Fig. 8 shows a result after applying schemes provided by the present invention to the IC package (lead-on chip package) shown in Fig. 7.

Fig. 9 shows a wafer divided into a plurality of dice.

Fig. 10 shows a cross sectional view of a die placed onto a seating apparatus, to be reduced in size according to the present invention.

Fig. 11 shows a cross sectional view of a semiconductor unit placed onto a seating apparatus and being etched according to the present invention.

Fig. 12 shows a cross sectional view of a semiconductor unit placed onto a chip tray and having been etched, according to the present invention, to have a thickness reaching a specified range.

Fig. 13 shows a scheme of attaching, according to the present invention, a semiconductor unit to a carrier after moving the semiconductor unit out from a chip tray.

Fig. 14 shows another scheme of attaching, according to the present invention, a semiconductor unit to a carrier after moving the semiconductor unit out from a chip tray.

Fig. 15 shows a further scheme of attaching, according to the present invention, a semiconductor unit to a carrier after moving the semiconductor unit out from a chip tray.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 shows a main step (A) of a method provided by the present invention for reducing the size of at least a semiconductor unit.

According to Fig. 1, a semiconductor unit 25 includes a first surface 22 and a second surface 23, wherein second surface 23 has not yet been ground or has been so ground that the semiconductor unit 25 has its size approximating an expected specification such as a desired thickness, and the semiconductor unit 25 attaches to or electrically connects a carrier 21 such as a substrate via bump 24. For an example of the size of semiconductor unit 25 approximating the expected specification, the expected specification may be a thickness ranging from 2 mil to 6 mil, and the semiconductor unit 25 has been ground to have a thickness ranging between 8 mil and 10 mil.

Fig. 2 shows another main step (B) of a method provided by the present invention for reducing the size of at least a semiconductor unit. According to Fig. 2, semiconductor unit 25 is etched from second surface 23 by means 29 selected from among using a certain type of gas, or plasma, or beams of light.

To prevent etching process from affecting the quality or functions of carrier 21 and semiconductor unit 25 (to prevent the first surface 22 of semiconductor unit 25 or the bump 24 from being etched, for example), an embodiment shown in Fig. 3 is preferred. In Fig. 3, a fixture 26 is used to properly shield carrier 21 and semiconductor unit 25. For example, most part of carrier 21, the first surface 22 of semiconductor unit 25, and the bump 24 in Fig. 3 are shielded by fixture 26, and thereby are immunized against etching, whereby etching process can take effect only on the second surface 23 of semiconductor unit 25, as can be seen from Fig. 4.

Fig. 5 depicts the semiconductor unit 25 having been etched according to Fig. 4 to have a size meeting an expected specification, and therefore requiring no more etching. For example, the expected

specification is a thickness ranging between 2 mil and 6 mil and measured relative to the first surface 22, and the semiconductor unit 25 needs no more etching when its thickness measured relative to surface 22 reaches the range which is between 2 mil and 6 mil. More is to be depicted according to Fig. 6.

As the size of semiconductor unit 25 in Fig. 5 has met the expected specification, fixture 26 is moved away, and a package including semiconductor unit 25 and carrier 21 is thus obtained, as shown in Fig. 6. In Fig. 6, the thickness of semiconductor unit 25 meeting the expected specification is indicated by 28 which, based on the above example, is between 2 mil and 6 mil.

The method provided by the present invention and defined according to Figs. 3 ~ 5 may also be applied to the package structure (lead-on chip package) shown in Fig. 7. Fig. 7 differs from Fig. 1 in that the semiconductor unit 75 in fig. 7 is a wire bonding chip stuck to carrier 71 via adhesive material. Just shield the carrier 71 and semiconductor unit 75 shown in Fig. 7 according to the same way as shown in Fig. 3, the etching process can take effect only on the second surface 73 of semiconductor unit 75, and the steps defined by Fig. 4 ~6 can also be applicable to size reduction of the semiconductor unit shown in Fig. 7 for obtaining a package structure shown in Fig. 8.

The bonding wire 76 in Fig. 7 may be installed to electrically connect semiconductor unit 75 and carrier 71 after the etching process and the removal of fixture, or before the etching process if it can be immunized against the etching process.

Another aspect of the method provided by the present invention for reducing the size of at least a semiconductor unit may be depicted by the embodiments shown in Fig. 9 ~ 15. In Fig. 9, a wafer is divided into a

plurality of dice among which at least a die 80 has its size to be reduced according to a method provided by the present invention. Figs. 10 ~ 12 show essential steps provided by the present invention for reducing the size of at least a die 80 shown in Fig. 9.

In Fig. 10, die 80 is attached to a seating apparatus 91 (a chip tray, for example) or an apparatus including a suitable tray onto which die 80 may be placed, or a carrier such as a chip carrier mechanically and/or electrically connectible with the semiconductor unit 80, the first surface 81 of the semiconductor unit (die 80) faces the seating apparatus and the second surface 82 thereof is exposed. As shown in Fig. 11, semiconductor unit (die 80) is etched from its second surface 82 by means 89 until its size meets an expected specification. For example, when the thickness of the semiconductor unit 80 measured relative to its first surface 81 becomes to be within a range of 2 mil ~ 6 mil, the etching process ends, as may be represented by Fig. 12. The etched semiconductor unit 80 in Fig. 12 is then moved out from apparatus 91 to stick to a carrier 121 via its second surface 82 as shown in Fig. 13 if the semiconductor unit 80 connects a carrier in a conventional mode, or to have its first surface 81 connected to a carrier 121 via bump 84 as shown in Fig. 14 if the semiconductor unit 80 is a flip chip, or to have its first surface 81 stuck to carrier 121 and its electrical connection device 83 (located on first surface 81) exposed to an opening 122 of carrier 121 as shown in Fig. 15 if the semiconductor unit 80 is to be packaged in a structure of Lead On Chip. In case the seating apparatus is a carrier mechanically and/or electrically connectible with the semiconductor unit 80, the semiconductor unit 80 may be connected to the seating apparatus before the etching process, and requires no steps of moving the semiconductor unit to another carrier after the etching process.

The etching process according to Fig. 11 may be implemented by means 89 of using a certain type of gas, or beams of light. A preferred embodiment according to the present invention is to etch the semiconductor unit 80 by means of using plasma. The expected specification in the above embodiments may mean that the thickness of the semiconductor unit 80 measured relative to the first surface 81 is within a specified range (between 2 mil and 6 mil, for example). The first surface 81 in Fig. 11 is immunized against the etching process by the shielding provided by the seating apparatus 91.

In the above embodiments of the present invention, if the initial size of the semiconductor unit is much larger than the expected specification (initial thickness is much larger than 10 mil while expected thickness is 6 mil, for example), a preferred embodiment of the method provided by the present invention for an application to packaging at least a semiconductor unit is to etch the semiconductor unit only after a step of reducing, on the basis of mechanical force such as grinding, the size of the semiconductor unit until the thickness of the semiconductor unit approximates the expected specification. For example, when the thickness reaches a range which spans from 8 mil to 10 mil.

While the invention has been described in terms of what are presently considered to be the most practical and preferred embodiments, it is to be understood that the invention needs not be limited to the disclosed embodiment. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims which are to be accorded with the broadest interpretation so as to encompass all such modifications and similar structures.

WHAT IS CLAIMED IS:

1. A method for reducing the size of at least a semiconductor unit in a process of packaging said semiconductor unit, comprising the steps of:

(A) attaching at least a part of a first surface of said semiconductor unit to a carrier; and

(B) etching said semiconductor unit from a second surface of said semiconductor unit until the size of said semiconductor unit meets an expected specification.

2. The method according to claim 1 wherein said semiconductor unit is etched by means selected from among using gas and using beams of light.

3. The method according to claim 1 wherein said semiconductor unit is etched by using plasma.

4. The method according to claim 1 wherein said expected specification means that the thickness of said semiconductor unit measured relative to said first surface is within a specified range.

5. The method according to claim 4 wherein said specified range is the range spanning between 2 mil and 6 mil.

6. The method according to claim 1 wherein step (B) comprises a step of shielding at least a part of said semiconductor unit and said carrier to prevent said etching from affecting the quality of said semiconductor unit and said carrier.

7. The method according to claim 1 further comprising, before step (A), a step of grinding said semiconductor unit until the size thereof approximates said expected specification.

8. The method according to claim 1 wherein step (B) comprises a step of using a fixture to shield at least a part of said semiconductor unit and said carrier for preventing said etching from affecting the quality

of said semiconductor unit and said carrier.

9. The method according to claim 1 wherein said semiconductor unit is attached to said carrier according to a configuration selected from among bump connection and lead-on chip packaging.

10. The method according to claim 1 wherein said carrier is selected from among a chip tray and a chip carrier, and said semiconductor unit includes at least a semiconductor electrical connection device located on said first surface.

11. A method for reducing the size of at least a semiconductor unit in a process of packaging said semiconductor unit wherein said semiconductor unit includes a first surface, a second surface, and at least a semiconductor electrical connection device located on said first surface, said method comprising the steps of:

(A) attaching said semiconductor unit to a seating apparatus, with said first surface facing said seating apparatus and said second surface exposed; and

(B) etching said semiconductor unit from said second surface until the size of said semiconductor unit meets an expected specification.

12. The method according to claim 11 wherein said semiconductor unit is etched by means selected from among using gas, beams of light, and plasma.

13. The method according to claim 11 further comprising, before step (A), a step of grinding said semiconductor unit until the size of said semiconductor unit approximates said expected specification.

14. The method according to claim 11 wherein said seating apparatus is selected from among a chip tray, and a chip carrier connectible with said semiconductor unit; and wherein said expected specification means that the thickness of said semiconductor unit measured

relative to said first surface is within a specified range.

15. The method according to claim 11 wherein said first surface is prevented by said seating apparatus from being etched.

16. The method according to claim 11 further comprising a step of moving said semiconductor unit from said seating apparatus to a carrier with said second surface attaching to said carrier via adhesive material.

17. The method according to claim 11 further comprising a step of moving said semiconductor unit from said seating apparatus to a carrier with said first surface attaching to said carrier via at least a bump.

18. The method according to claim 11 further comprising a step of moving said semiconductor unit from said seating apparatus to a carrier for forming a lead-on chip package.

19. A method for reducing the size of at least a semiconductor unit in a process of packaging said semiconductor unit wherein said semiconductor unit includes a first surface, a second surface, and at least a semiconductor electrical connection device located on said first surface, said method comprising the steps of:

dividing a wafer into a plurality of dice;

placing at least one die of said dice onto a seating apparatus, with said second surface exposed;

etching said die from said second surface, with said first surface shielded by said seating apparatus and thereby immunized against etching;

ending etching said die when the size of said die meets a predetermined specification, and moving said die from said seating apparatus to a chip carrier.

20. The method according to claim 19 wherein said seating apparatus includes a tray which said first surface is in, said predetermined specification means that the thickness of said die measured relative to said first surface is within a predetermined range, and when said die is moved to said chip carrier, said die attaches to said chip carrier in a way selected from among connecting said chip carrier via said first surface and connecting said chip carrier via said second surface according to the type of electrical connection between said die and said chip carrier.

METHOD FOR REDUCING SIZE OF SEMICONDUCTOR UNIT IN PACKAGING PROCESS

ABSTRACT OF THE DISCLOSURE

The present invention provides different schemes for reducing the size (such as thickness) of at least a semiconductor unit (such as an IC chip) which is to be packaged. It replaces, in packaging at least a semiconductor unit, conventional grinding processes by etching schemes, particularly when the thickness of the semiconductor unit approximates an expected specification. The etching process may be embodied in a way that a semiconductor unit attached to a carrier such as a substrate, or placed onto a seating apparatus such as a chip tray, and properly shielded, is etched by means of using gas such as plasma, or beams of light. The semiconductor unit packaged according to the scheme provided by the present invention can thus be immunized against the failure resulting from die crack or back-side chipping.

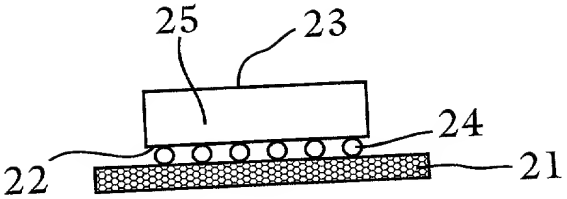

Fig. 1

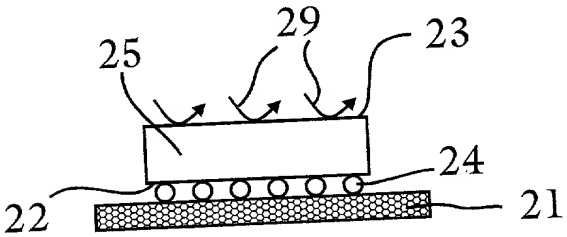

Fig. 2

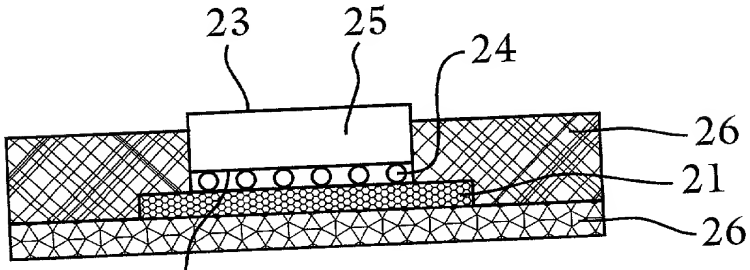

Fig. 3

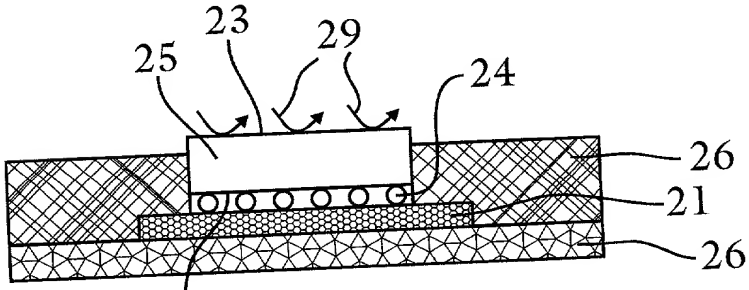

Fig. 4

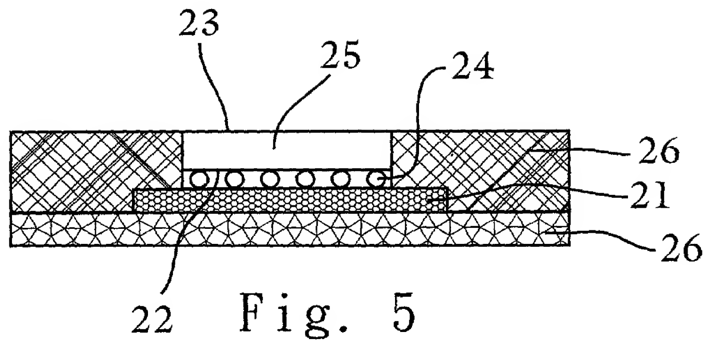

Fig. 5

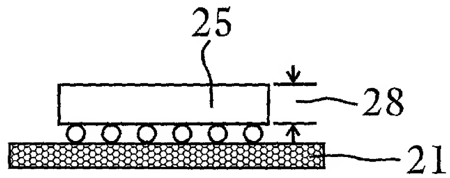

Fig. 6

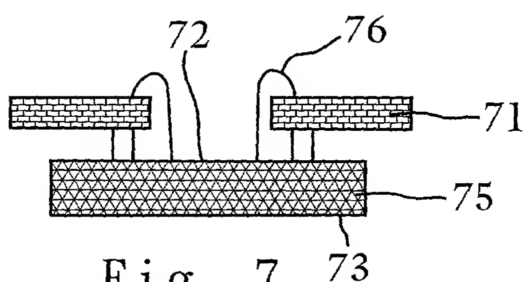

Fig. 7

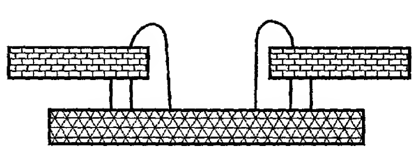

Fig. 8

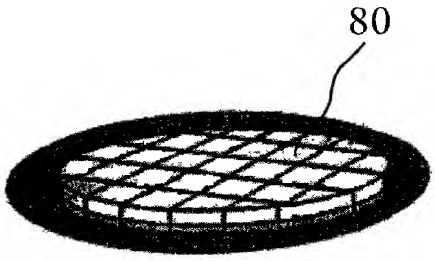

Fig. 9

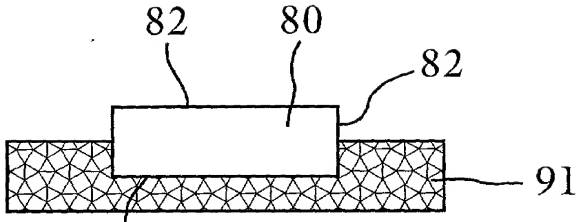

Fig. 10

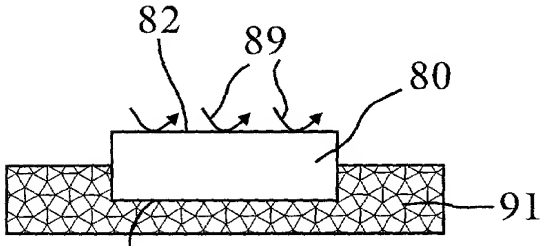

Fig. 11

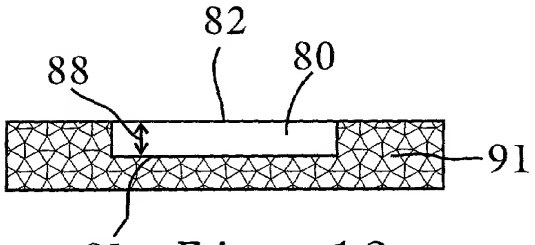

Fig. 12

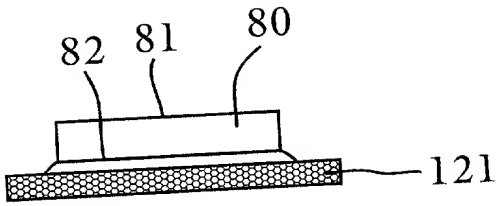

Fig. 13

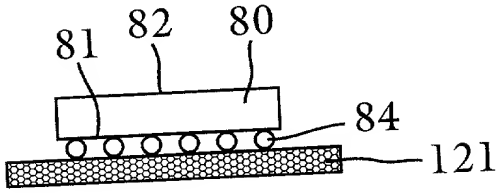

Fig. 14

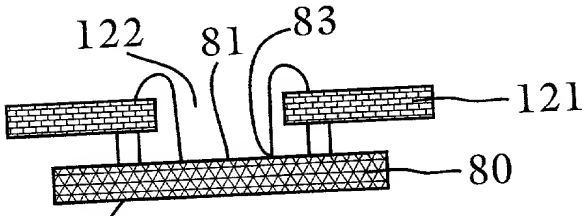

Fig. 15

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COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled <METHOD FOR REDUCING SIZE OF SEMICONDUCTOR UNIT IN PACKAGING PROCESS>, the specification of which

[x] is attached hereto.

[ ] was filed on _____ as Application No. _____.

[ ] was described and claimed in PCT International Application No. _____, filed on _____, and as amended under PCT Article 19 on _____ (if applicable).

[ ] and was amended on _____ (if applicable).

[ ] with amendments through _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56. If this is a continuation-in-part application filed under the conditions specified in 35 U.S.C. § 120 which discloses and claims subject matter in addition to that disclosed in the prior copending application, I further acknowledge the duty to disclose material information as defined in 37 C.F.R. § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or of any PCT International application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT International application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
_____	_____	_____	[ ]	[×]
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

_____	_____
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of any PCT International application(s) designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United

States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT International filing date of this application:

(Application No.)	(Filing Date)	(Status: patented, Pending, abandoned)

The undersigned hereby authorizes the U.S. attorney or agent named herein to accept and follow instructions from I & A Consulting Co., Ltd / IA Office as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorney or agent named herein will be so notified by the undersigned.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application, and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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